In the Claims

Claims 34-47 (canceled).

Claim 1 (currently amended): A magnetoresistive memory device, comprising:

a memory bit comprising a stack which includes a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bit storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line proximate the stack and configured for utilization in reading information from the memory bit; ~~and~~

a second conductive line spaced from the stack by a greater distance than any distance which the first conductive line is spaced from the stack, and configured for utilization in writing information to the memory bit; and

wherein the first and second conductive lines extend longitudinally parallel to one another.

Claim 2 (original): The device of claim 1 wherein the first conductive line is in ohmic electrical contact with at least one of the magnetic layers of the memory bit, and wherein the second conductive line is not in ohmic electrical contact with either of the magnetic layers of the memory bit.

Claim 3 (original): The device of claim 1 wherein the first and second magnetic layers comprise one or more of nickel, iron, cobalt, iridium, manganese, platinum and ruthenium.

Claim 4 (original): The device of claim 1 wherein the non-magnetic layer comprises an electrically insulative material.

Claim 5 (original): The device of claim 1 wherein the non-magnetic layer comprises an electrically conductive material.

Claim 6 (original): The device of claim 1 wherein the first conductive line physically contacts one of the first and second magnetic layers.

Claim 7 (original): The device of claim 1 further comprising an electrically insulative material between the first and second conductive lines; and wherein the second conductive line is spaced from the stack by at least a combined thickness of the electrically insulative material and the first conductive line.

Claim 8 (original): The device of claim 7 wherein the electrically insulative material comprises a layer which includes one or both of silicon dioxide and silicon nitride, and which is at least about 100Å thick.

Claim 9 (original): The device of claim 1 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stack by at least a combined thickness of the electrically insulative material and the first conductive line; and

the first conductive line physically contacts one of the first and second magnetic layers.

Claim 10 (original): The device of claim 1 further comprising a third conductive line proximate the stack; the third conductive line being configured for utilization in both writing information to the memory bit and reading information from the memory bit.

Claim 11 (original): The device of claim 10 wherein the first conductive line physically contacts one of the first and second magnetic layers, and wherein the third conductive line physically contacts the other of the first and second magnetic layers.

Claim 12 (original): The device of claim 10 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stack by at least a combined thickness of the electrically insulative material and the first conductive line;

the first conductive line physically contacts one of the first and second magnetic layers; and

the third conductive line physically contacts the other of the first and second magnetic layers.

Claim 13 (currently amended): A magnetoresistive memory device, comprising:

a memory bit comprising a stack which includes a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bit storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line configured for utilization in reading information from the memory bit and in ohmic electrical contact with at least one of the magnetic layers; ~~and~~

a second conductive line configured for utilization in writing information to the memory bit and not in ohmic electrical contact with either of the magnetic layers of the memory bit; and

wherein the first and second conductive lines extend longitudinally parallel to one another.

Claim 14 (original): The device of claim 13 wherein the first conductive line physically contacts one of the first and second magnetic layers.

Claim 15 (currently amended): A magnetoresistive memory device, comprising:

a stack comprising a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers;

a first conductive line over the stack and configured to generate an electrical field which sufficiently overlaps at least a first portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

a second conductive line under the stack and configured to generate an electrical field which sufficiently overlaps at least a second portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

an electrically insulative spacer under the second conductive line; ~~and~~

a third conductive line under the insulative spacer and spaced from the second conductive line by at least the insulative spacer; the third conductive line being configured to generate an electrical field which sufficiently overlaps at least a third portion of the stack to alter a magnetic orientation within at least one of the magnetic layers; and

wherein the second and third conductive lines extend longitudinally parallel to one another.

Claim 16 (original): The device of claim 15 wherein the first, second and third conductive lines alter a magnetic orientation within the same one of the two magnetic layers, and do not alter a magnetic orientation of the other of the two magnetic layers.

Claim 17 (original): The device of claim 15 wherein the first and second magnetic layers comprise one or more of nickel, iron, cobalt, iridium, manganese, platinum and ruthenium.

Claim 18 (original): The device of claim 15 wherein the non-magnetic layer comprises an electrically insulative material.

Claim 19 (original): The device of claim 15 wherein the non-magnetic layer comprises aluminum oxide.

Claim 20 (original): The device of claim 15 wherein the non-magnetic layer comprises an electrically conductive material.

Claim 21 (original): The device of claim 15 wherein the non-magnetic layer comprises copper.

Claim 22 (original): The device of claim 15 wherein the first conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the first conductive line to a level of from about 1 milliamp to about 10 milliamps.

Claim 23 (original): The device of claim 15 wherein the second conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the second conductive line to a level of from about 500 nanoamps to about 1 microamp.

Claim 24 (original): The device of claim 15 wherein the third conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the third conductive line to a level of from about 1 milliamp to about 10 milliamps.

Claim 25 (original): The device of claim 15 wherein:

the first conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the first conductive line to a level of from about 1 milliamp to about 10 milliamps;

the second conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the second conductive line to a level of from about 500 nanoamps to about 1 microamp; and

the third conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the third conductive line to a level of from about 1 milliamp to about 10 milliamps.

Claim 26 (currently amended): A magnetoresistive memory device assembly, comprising:

an array comprising a plurality of individual memory bits; the memory bits including a stack having a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bits storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line extending across a first set comprising several of the individual memory bits of the array; the first conductive line being proximate the stacks of the first set of the individual memory bits of the array and configured for utilization in reading information from the memory bits;

a second conductive line extending across the first set of the memory bits of the array and spaced from the stacks of the first set of the individual memory bits by a greater distance than any distance which the first conductive line is spaced from the stacks; the second conductive line being configured for utilization in writing information to the memory bits;

a first transistor electrically connected with the first set of the individual memory bits of the array through the first conductive line; ~~and~~

a second transistor electrically connected with the first set of the individual memory bits of the array through the second conductive line; and

wherein the first and second conductive lines extend longitudinally parallel to one another.

Claim 27 (original): The assembly of claim 26 wherein the array comprises a footprint over a supporting substrate, and wherein the first and second transistors are peripheral to the footprint of the array.

Claim 28 (original): The assembly of claim 26 further comprising an electrically insulative material between the first and second conductive lines; and wherein the second conductive line is spaced from the stacks of the first set of the individual memory bits by at least a combined thickness of the electrically insulative material and the first conductive line.

Claim 29 (original): The assembly of claim 26 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stacks of the first set of the individual memory bits by at least a combined thickness of the electrically insulative material and the first conductive line; and

the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits.

Claim 30 (original): The assembly of claim 26 further comprising a third conductive line proximate at least one memory bit of the first set of the individual memory bits; the third conductive line being configured for utilization in both writing information to the at least one memory bit and reading information from the at least one memory bit.

Claim 31 (original): The assembly of claim 30 wherein the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits; and wherein the third conductive line physically contacts the other of the first and second magnetic layers.

Claim 32 (original): The assembly of claim 30 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stacks of the first set of the individual memory bits by at least a combined thickness of the electrically insulative material and the first conductive line;

the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits; and

and the third conductive line physically contacts the other of the first and second magnetic layers.

Claim 33 (original): The assembly of claim 30 further comprising a third transistor electrically connected with the at least one memory bit through the third conductive line.

Claim 48 (new): A magnetoresistive memory device, comprising:

a stack comprising a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers;

a first conductive line over the stack and configured to generate an electrical field which sufficiently overlaps at least a first portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

a second conductive line under the stack and configured to generate an electrical field which sufficiently overlaps at least a second portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

an electrically insulative spacer under the second conductive line;

a third conductive line under the insulative spacer and spaced from the second conductive line by at least the insulative spacer; the third conductive line being configured to generate an electrical field which sufficiently overlaps at least a third portion of the stack to alter a magnetic orientation within at least one of the magnetic layers; and

wherein the first conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the first conductive line to a level of from about 1 milliamp to about 10 milliamps.

Claim 49 (new): A magnetoresistive memory device, comprising:

a stack comprising a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers;

a first conductive line over the stack and configured to generate an electrical field which sufficiently overlaps at least a first portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

a second conductive line under the stack and configured to generate an electrical field which sufficiently overlaps at least a second portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

an electrically insulative spacer under the second conductive line;

a third conductive line under the insulative spacer and spaced from the second conductive line by at least the insulative spacer; the third conductive line being configured to generate an electrical field which sufficiently overlaps at least a third portion of the stack to alter a magnetic orientation within at least one of the magnetic layers; and

wherein the second conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the second conductive line to a level of from about 500 nanoamps to about 1 microamp.

Claim 50 (new): A magnetoresistive memory device, comprising:

a stack comprising a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers;

a first conductive line over the stack and configured to generate an electrical field which sufficiently overlaps at least a first portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

a second conductive line under the stack and configured to generate an electrical field which sufficiently overlaps at least a second portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

an electrically insulative spacer under the second conductive line;

a third conductive line under the insulative spacer and spaced from the second conductive line by at least the insulative spacer; the third conductive line being configured to generate an electrical field which sufficiently overlaps at least a third portion of the stack to alter a magnetic orientation within at least one of the magnetic layers; and

wherein the third conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the third conductive line to a level of from about 1 milliamp to about 10 milliamps

Claim 51 (new): A magnetoresistive memory device, comprising:

a stack comprising a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers;

a first conductive line over the stack and configured to generate an electrical field which sufficiently overlaps at least a first portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

a second conductive line under the stack and configured to generate an electrical field which sufficiently overlaps at least a second portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

an electrically insulative spacer under the second conductive line;

a third conductive line under the insulative spacer and spaced from the second conductive line by at least the insulative spacer; the third conductive line being configured to generate an electrical field which sufficiently overlaps at least a third portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

wherein the first conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the first conductive line to a level of from about 1 milliamp to about 10 milliamps;

wherein the second conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the second conductive line to a level of from about 500 nanoamps to about 1 microamp; and

wherein the third conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the third conductive line to a level of from about 1 milliamp to about 10 milliamps.

Claim 52 (new): A magnetoresistive memory device assembly, comprising:

an array comprising a plurality of individual memory bits; the memory bits including a stack having a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bits storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line extending across a first set comprising several of the individual memory bits of the array; the first conductive line being proximate the stacks of the first set of the individual memory bits of the array and configured for utilization in reading information from the memory bits;

a second conductive line extending across the first set of the memory bits of the array and spaced from the stacks of the first set of the individual memory bits by a greater distance than any distance which the first conductive line is spaced from the stacks; the second conductive line being configured for utilization in writing information to the memory bits;

a first transistor electrically connected with the first set of the individual memory bits of the array through the first conductive line;

a second transistor electrically connected with the first set of the individual memory bits of the array through the second conductive line; and

a third conductive line proximate at least one memory bit of the first set of the individual memory bits; the third conductive line being configured for utilization in both

writing information to the at least one memory bit and reading information from the at least one memory bit.

Claim 53 (new): The assembly of claim 52 wherein the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits; and wherein the third conductive line physically contacts the other of the first and second magnetic layers.

Claim 54 (new): The assembly of claim 52 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stacks of the first set of the individual memory bits by at least a combined thickness of the electrically insulative material and the first conductive line;

the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits; and

and the third conductive line physically contacts the other of the first and second magnetic layers.

Claim 55 (new): The assembly of claim 52 further comprising a third transistor electrically connected with the at least one memory bit through the third conductive line.